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Digital & Microprocessor Electronics

Digital Circuit Fundamentals 2

FACET®

Student Workbook

91576-00
Edition 4

3091576000503

FOURTH EDITION

Second Printing, March 2005

ISBN 0-86657-214-7

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LAB-VOLT SYSTEMS, INC.
P.O. Box 686
Farmingdale, NJ 07727
Attention: Program Development
Phone: (732) 938-2000 or (800) LAB-VOLT
Fax: (732) 774-8573
Technical Support: (800) 522-4436
Technical Support E-Mail: techsupport@labvolt.com

Table of Contents

Introduction

This Student Workbook provides a unit-by-unit outline of the Fault Assisted Circuits for Electronics Training (F.A.C.E.T) curriculum.

The following information is included together with space to take notes as you move through the curriculum.

- The unit objective
- Unit fundamentals
- A list of new terms and words for the unit
- Equipment required for the unit
- The exercise objectives
- Exercise discussion
- Exercise notes

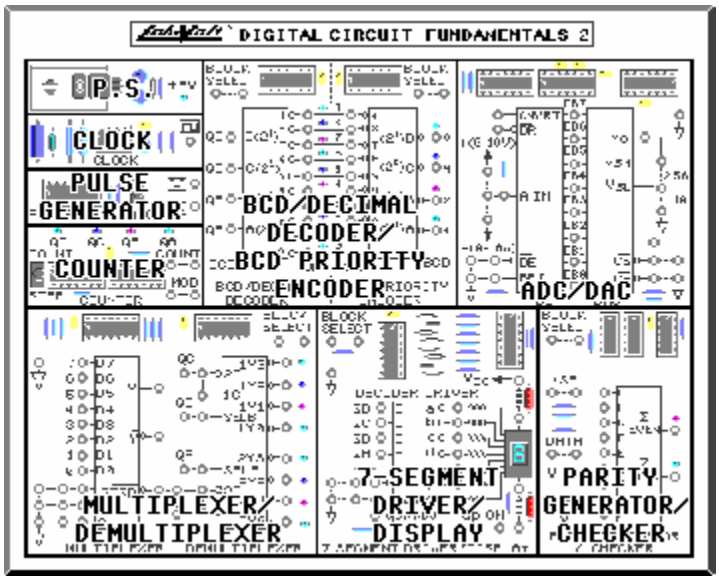
The **Appendix** includes safety information.

UNIT 1 – CIRCUIT BOARD FAMILIARIZATION

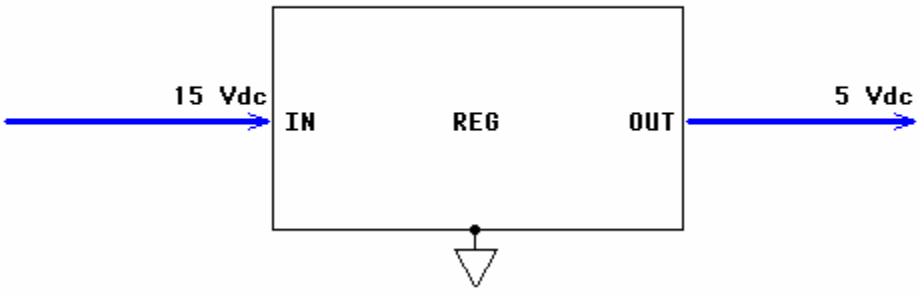
UNIT OBJECTIVE

At the completion of this unit, you will be able to identify and operate the circuit blocks on the DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board.

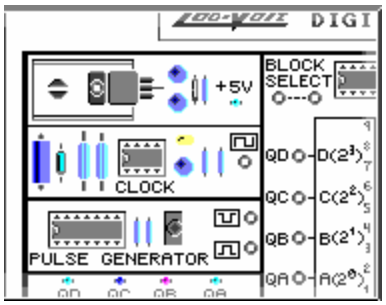
UNIT FUNDAMENTALS



The DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board consists of 6 training circuit blocks. A general purpose circuit block consists of a 5V regulator, a square wave clock generator, a pulse generator, and a 4-bit counter.

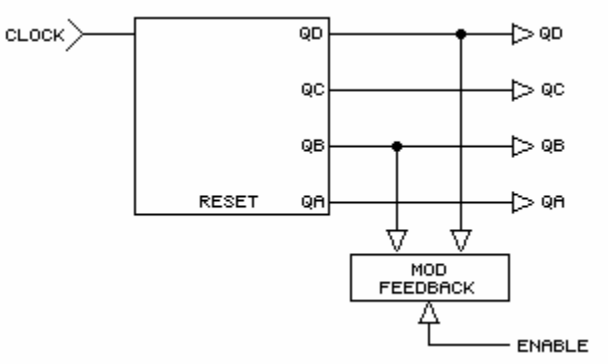


A **voltage regulator** converts the system's 15 Vdc power supply to 5 Vdc, required by the **integrated circuits (ICs)** on the circuit board. Power supply voltages are **hardwired** to all devices of the circuit board.



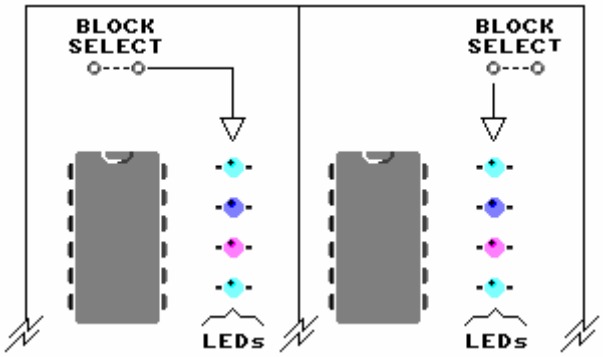
The 555 **timer** CLOCK circuit generates a square waveform, useful as an input signal generator.

The PULSE GENERATOR circuit's toggle switch generates positive-and negative-going signal edges. The "at home" position of this toggle switch is up.



The COUNTER circuit generates a 4-bit output with a count value between 0 and 15 (1111 in binary form).

If **MOD** is enabled, the counter modulus is 10 (output between 0 and 9). You can free-run or step the counter outputs (QD, QC, QB, and QA).



Placement of two-post connectors and interconnecting leads activates various circuit functions and connects circuit blocks. Inserting a two-post connector in the BLOCK SELECT terminals, for example, powers specific LED circuits.

ICs are mounted in dual-in-line sockets and are of the **TTLLS**(74LSxx family) type. The **DAC**and **ADC**use I^2L (integrated injection logic) technology.

Decoupling capacitors, which bypass ICs, and pull-up resistors, which determine logic levels, are incorporated into the design.

NEW TERMS AND WORDS

voltage regulator - an IC that maintains a constant output voltage when input voltage and output loads change.
integrated circuits (ICs) - devices that combine the actions of many transistors on one chip.
hardwired - refers to connections made in copper on a printed circuit board as opposed to connections that must be completed with a wire or test load.
timer - IC (555 type) used in conjunction with external components to generate various waveforms, such as a pulse train.
MOD - the modulus of a counter; a circuit feedback used to set the maximum output value of a counter.
TTL - transistor-transistor logic.
LS - low power Schottky; a logic family that has high speed but low power consumption.
DAC - digital to analog converter; an IC that converts digital inputs to an equivalent analog output.
ADC - analog to digital converter; an IC that converts analog inputs to an equivalent digital output.
decoupling capacitors - a capacitor that reduces the impedance between the power supply bus and the IC that the bus powers.
pulse train - a free-running and repetitive waveform, usually refers to a square waveform.
dual-in-line packages (DIPs) - types of IC packages that have the same number of pins on both sides of the devices.

EQUIPMENT REQUIRED

F.A.C.E.T. base unit
Multimeter
Oscilloscope, dual trace
DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board

NOTES

Exercise 1 – Component Location and Identification

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to locate the major circuit blocks of the circuit board. You will verify your results by correctly identifying circuits and their major components.

DISCUSSION

- Discuss modifying circuit configurations with two-post connectors.
- Observe that test points and/or LEDs are provided for voltage level verification.

NOTES

Exercise 2 – Operation of the General Circuits

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to use the general purpose circuits of the circuit board. You will verify your knowledge by taking voltage and waveform readings.

DISCUSSION

- Discuss the four general purpose circuits on the circuit board.

NOTES

Exercise 3 – IC Package Fundamentals

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to determine IC pin locations for LS devices. You will verify your results by using the circuit board.

DISCUSSION

- Discuss physical characteristics of the board mounted ICs.
- Discuss general electrical characteristics of board mounted ICs.

NOTES

UNIT 2 – DECODER AND PRIORITY ENCODER

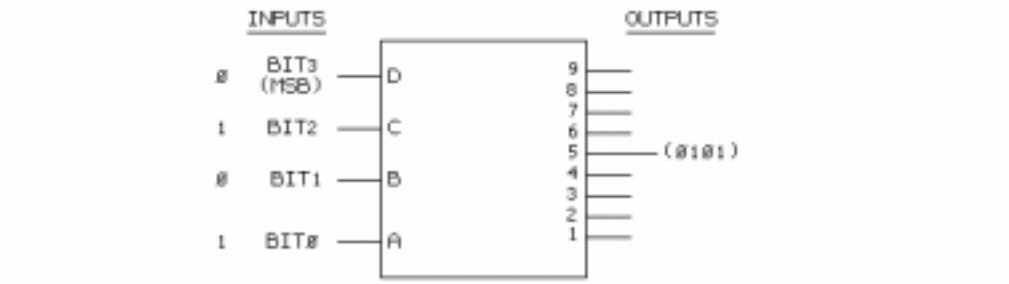
UNIT OBJECTIVE

At the completion of this unit, you will be able to locate, operate, and control a decoder and encoder circuit combination.

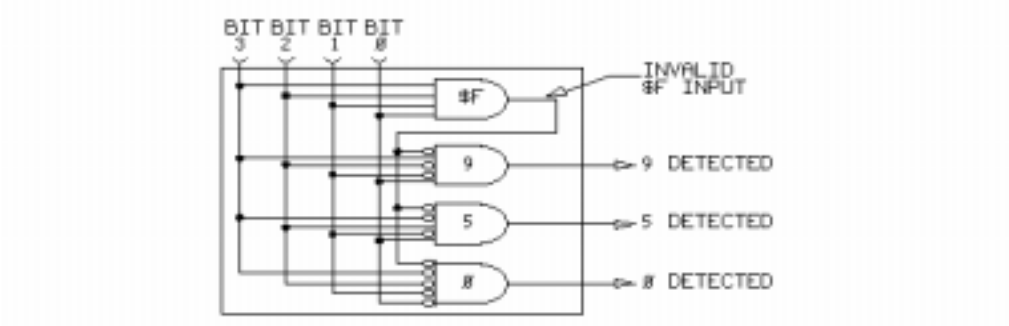
UNIT FUNDAMENTALS

BCD BIT CODE	DECIMAL VALUE
1111 THROUGH 1010	INVALID CODES IN BCD FORMAT
1001	9
1000	8
0111	7
0110	6
0101	5
0100	4
0011	3
0010	2
0001	1
0000	0

A **binary coded decimal** (BCD) **decoder** detects and indicates unique 8-4-2-1 bit combinations between 0 and 9 decimal, or **base** 10 (indicated by 9_{10}). BCD information ranges between 0 and 9. Codes above 9 (10 through 15 for a 4-bit word) are invalid. These bit patterns are usually not decoded but generate some form of "out of limit" indication.

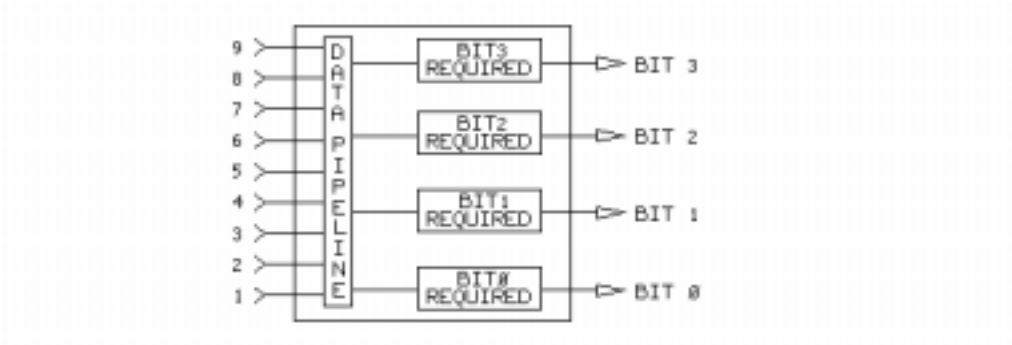


In the BCD decoder, only one output is active for a given input bit group. The active state can be high or low depending on the type of IC selected. A 4-bit BCD input activates one of the outputs (0101 activates 5, for example).

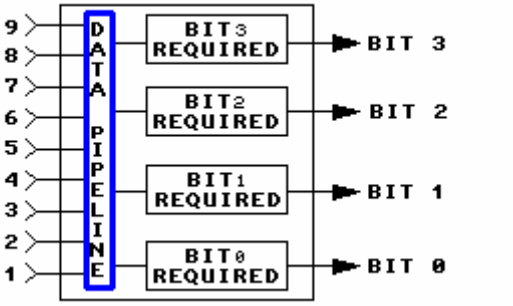


Each decoder section detects a specific input bit code. In this example, section 0 detects a 0000 input. Section 5 detects a 0101 input. Section 9 detects a 1001 input.

A binary-coded decimal **encoder** reverses the process of the BCD decoder. The encoder detects inputs between 9_{10} and 0 and generates unique 4-bit BCD codes. Because the encoder outputs represent BCD equivalents, more than one output at a time may be active.

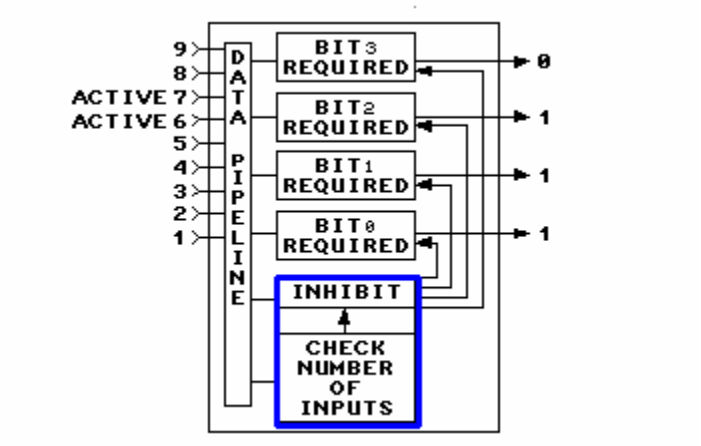


A BCD encoder has nine possible active inputs, 1 through 9. A 0 input is not required because inactive inputs generate inactive outputs.



Each bit section of an encoder is connected to a **data pipeline**, which distributes the input data. Each section decides if its bit is required to represent part of the 4-bit BCD code. If a specific bit is needed, that section activates its output. If a specific bit is not needed, that section deactivates its output. For example, an input of 6 requires a BCD output of 0110; therefore, sections BIT2 and BIT1 are active, and sections BIT3 and BIT0 are inactive.

Each encoder input represents a unique BCD code; therefore, two or more active inputs should cause an output error. If inputs 6 (0110) and 7 (0111) are both active, BIT0 cannot be inactive (xxx0) and active (xxx1) simultaneously.



Encoders use another operating section to determine input priority (called **priority detection**). Detecting more that one input activates the INHIBIT section. This section ensures that only output bits associated with the **higher** input value are encoded. Lower input values are locked out.

NEW TERMS AND WORDS

binary coded decimal - (BCD) a form of 4-bit coding representing decimal number between 9 and 0.
decoder - a circuit that generates one unique output in response to a set of input bit patterns.
base - indicates the numbering system; base 10 indicates decimal, base 2 indicates binary, and base 16 indicates hexadecimal.
disables - turns off, deactivates, inhibits, or makes nonresponsive.
enables - turns on, activates, or makes responsive.
encoder - a circuit that generates unique output bit patterns in response to a specific input.
data pipeline - a common data path used to distribute information throughout a circuit.

EQUIPMENT REQUIRED

F.A.C.E.T. base unit
Multimeter
Oscilloscope, dual trace
DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board

NOTES

Exercise 1 – BCD Decoder Operation

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to operate a BCD to decimal decoder. You will verify your results by decoding 4-bit word inputs.

DISCUSSION

- Discuss the electronic functions of the 74LS42 BCD to decimal decoder.

NOTES

Exercise 2 – Priority Encoder Operation

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to operate a decimal input priority encoder. You will verify your results by encoding decimal inputs.

DISCUSSION

- Discuss the electronic functions of the 74LS147 BCD to decimal encoder.

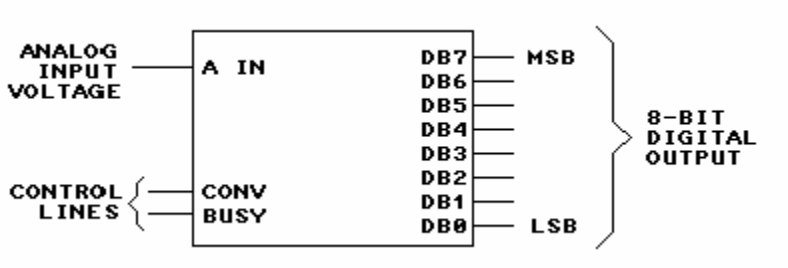
NOTES

UNIT 3 – ADC AND DAC OPERATION

UNIT OBJECTIVE

At the completion of this unit, you will be able to identify, operate, and control ADC and DAC circuits.

UNIT FUNDAMENTALS



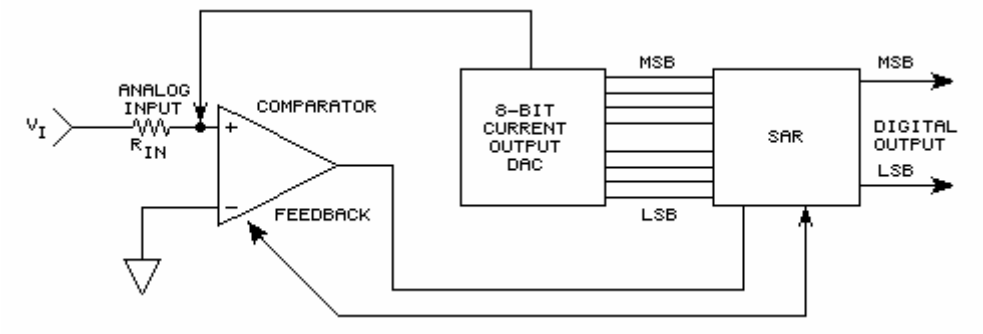
An **analog to digital converter** (ADC) generates a digital output code equivalent to the value of an analog input voltage. The analog input voltage is converted into an 8-bit digital output.

Generally, the digital output codes range from $00 through $FF (binary 0000 0000 through 1111 1111). DB7 is the most significant bit (MSB) of the ADC output, and DB0 is the least significant bit (LSB).

Binary numbers, such as 1010 0101, are written with the MSB at the left side.

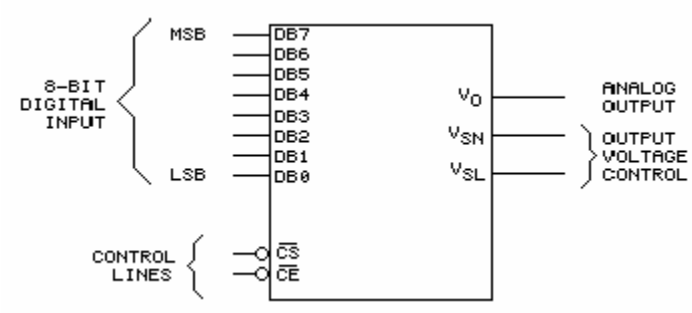
MSB				LSB			
1	0	1	0	0	1	0	1

For the ADC used on your circuit board, input voltage is either **unipolar** or **bipolar**. A unipolar input voltage ranges from 0 through +10 Vdc and generates an output code from $00 to $FF, respectively. Mid-scale occurs at 5 Vdc. A bipolar input voltage ranges from -5 Vdc through +5 Vdc and also generates an output code from $00 to $FF, respectively. However, mid- scale occurs at 0 Vdc.



The AD673 ADC studied in this unit uses a **successive approximation register** (SAR) to process an analog input voltage. An SAR essentially compares two currents and in the process of making the currents identical, generates the ADC 8-bit output.

An SAR conversion circuit has a comparator, an 8-bit current output DAC, and the SAR register. The comparator output stimulates the SAR to sequence the 8-bit current output DAC from MSB to LSB. At each bit point, a current is fed back to the comparator. If the **sum** value is greater than the input current, the respective bit is turned off; if the sum value is less, the respective bit is turned on. This process continues until 8 output bits are generated.



A **digital to analog converter** (DAC) generates an analog output voltage equivalent to the value of a binary code input. The 8-bit digital input is converted into an analog output. Generally, the digital input codes range from $00 through $FF (binary 0000 0000 through 1111 1111).

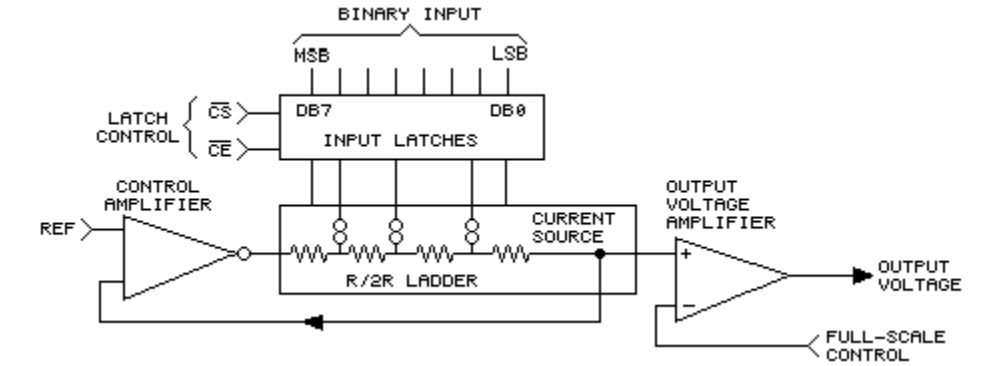
DB7 is the MSB of the DAC, and DB0 is the LSB.

Binary numbers, such as 1010 0101, are written with the MSB at the left side.

MSB LSB
1 0 1 0 0 1 0 1

V_{SN} and V_{SL} select a full-scale output voltage of 10 Vdc or 2.5 Vdc. A 10V full-scale output has a mid-scale value of about 5V. A 2.5V full-scale output has a mid-scale value of about 1.27V.

The AD558 DAC studied in this unit uses 8 **current sources** (3 are shown) switched into an **R/2R ladder** to process a digital binary input code. The current source and the R/2R ladder null the reference (REF) voltage and generate an analog output voltage in the process.



As current is switched into the R/2R ladder, a voltage drop is developed. The voltage drives the control amplifier and the output voltage amplifier.

The control amplifier buffers the internal **band-gap** reference voltage and controls the amplitude of current through the ladder. The input latches store the binary input codes.

NEW TERMS AND WORDS

analog to digital converter - an IC or process that generates a binary output code equivalent to the value of an analog input voltage.
unipolar - possessing one polarity (+) or (-) with respect to circuit common (zero).
bipolar - possessing positive (+) or negative (-) polarity with respect to circuit common (zero).
successive approximation register - a circuit, used in conjunction with a current output DAC, which generates a binary-coded output equivalent to the value of a current input.
digital to analog converter - an IC or process that generates an analog output voltage equivalent to the value of a binary input code.
current sources - a circuit designed to provide a fixed and stable current output.
R/2R ladder - a resistive network in which each resistor has a 2:1 (larger or smaller) relationship to the value of a binary input code.
band-gap - a very accurate and temperature-stable voltage reference source.

EQUIPMENT REQUIRED

F.A.C.E.T. base unit
Multimeter
Oscilloscope, dual trace
DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board

NOTES

Exercise 1 – ADC Operation

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to operate and predict the performance of an ADC. You will verify your knowledge by performing unipolar and bipolar conversions.

DISCUSSION

- The AD673 is an 8-bit output device that converts an analog input voltage to an equivalent 8-bit straight binary output code.
- The ADC has an LSB weight of about 39 mV.
- The outputs generate TTL levels.
- DE controls the tristate drivers.
- Bipolar select (BPI) determines the range of the analog input voltage.
- The AD673 ADC has a typical conversion interval of 20 μsec.

NOTES

Exercise 2 – DAC Operation

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to operate and predict the performance of a DAC. You will verify your knowledge by performing digital to analog conversions.

DISCUSSION

- The AD558 DAC is an 8-bit input device that converts a binary input code into equivalent analog output voltage.
- Circuit inputs provide a straight 8-bit DAC binary code.
- The LSB weight of your DAC is about 39 mV (10V full-scale) or about 10 mV (2.56V full-scale).
- The DAC output requires a typical settling time (output stable) of 0.8 μsec in its 2.56V full-scale configuration and 2 μsec in its 10V full-scale configuration.
- The DAC has data input latches, which are controlled by inputs CS and CE. The latches are transparent with CS and CE low.
- In the latched state, changes to the input data have no effect on the DAC output. The output data reflects the input data previously "latched" into the DAC.

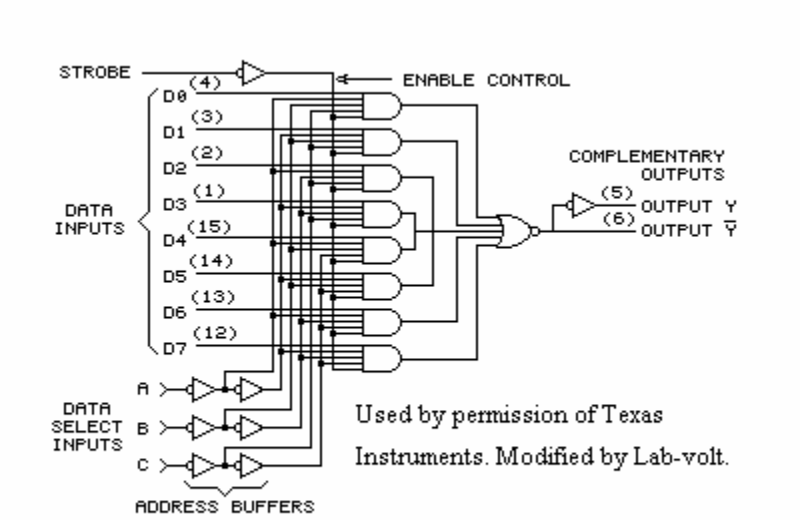
NOTES

UNIT 4 – MULTIPLEXER AND DEMULTIPLEXER

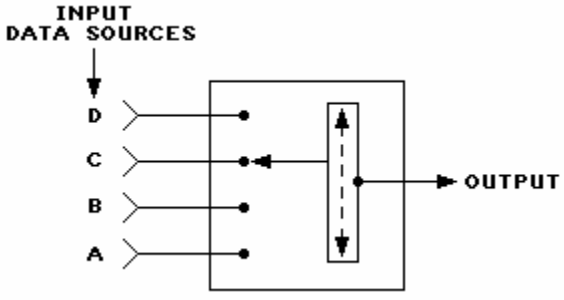
UNIT OBJECTIVE

At the completion of this unit, you will be able to operate and control a multiplexer and demultiplexer circuit.

UNIT FUNDAMENTALS

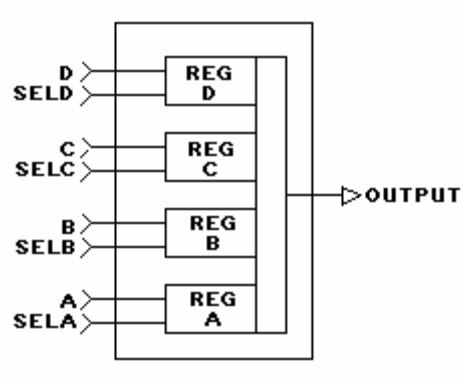


The 74LS151 **multiplexer** on your circuit board is a 1-of-8 data selector. It is an MSI device with a gate complexity of 17 equivalent gates.



A multiplexer allows the selection of one data source from a group. You can connect the output to any of the input data sources (A through D) by positioning the multiplexer pointer.

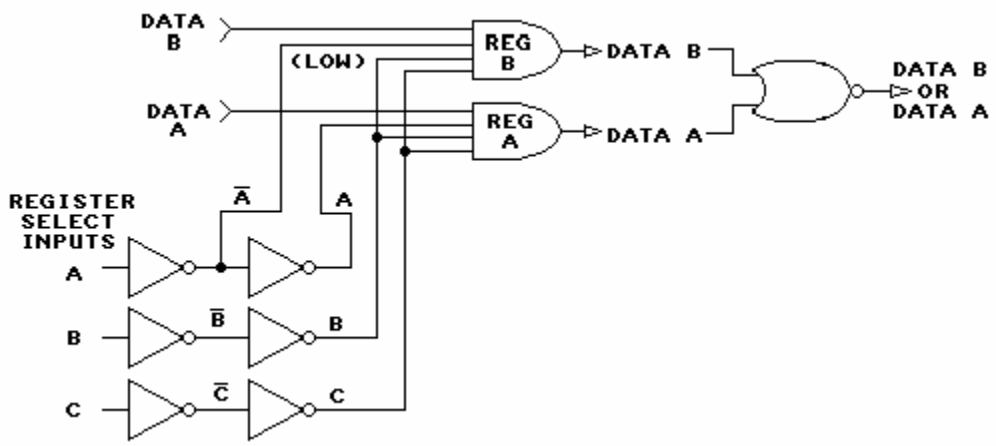
In this multiplexer, input data source C is selected. This input passes through the multiplexer pointer to the output. Data sources A, B, and D have no effect on the multiplexer output.



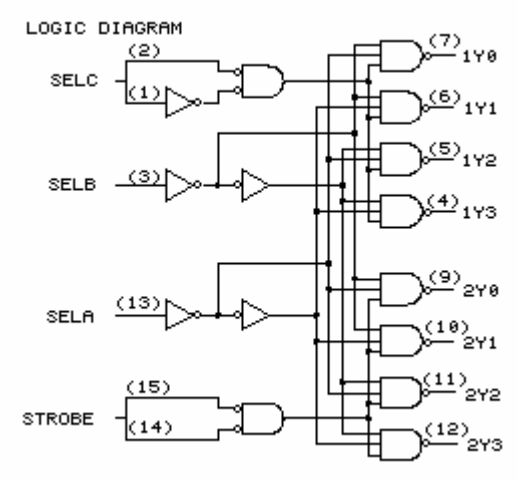
On the 74LS151 multiplexer, pointer movement is provided electrically through a register select process. Internal registers (REG) allow the selection of a specific data input. Each register is enabled by a select (SEL) line.

Part of the selection process deals with an output-enable control line called a **strobe (STRB)**. On the 74LS151, the strobe input disables or enables all data registers simultaneously.

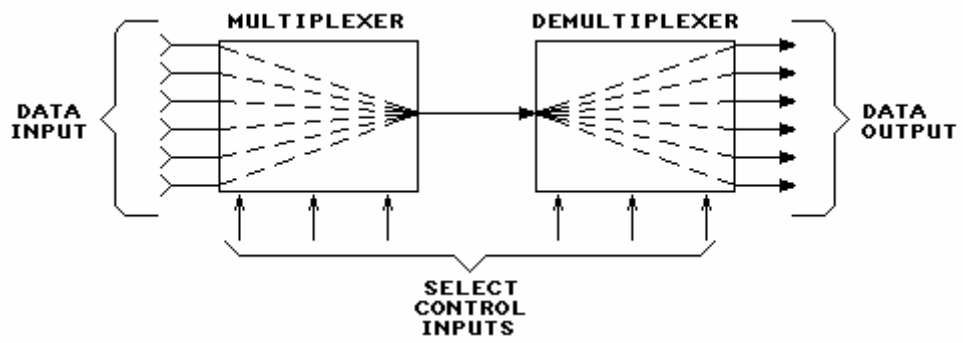
DATA A and SELA have no effect on the output if the STRB input is high. STRB high disables the output of REGISTER A. If STRB is low, the register is enabled, and DATA A can be passed
to the output.



This circuit illustrates two internal pathways of the 74LS151 multiplexer. Register A is enabled when the register select inputs equal binary 111. REG B is disabled because A is high and $\overline{A}$ is low.



The 74LS155 on your circuit board is a dual 2-4 line decoder configured as a 1-line-to-8-line data **demultiplexer**. It is an MSI device with a gate complexity of 15 equivalent gates.



The demultiplexer allows one data source to selectively drive individual elements of a group. In this demultiplexer, lines of data (data input) are multiplexed down to 1 line. In turn, the data on this line is placed on 1 of 6 lines.

NEW TERMS AND WORDS

multiplexer - a circuit that selectively connects one data line of a group to one output line.
strobe (STRB) - the input data line of a multiplexer or demultiplexer.
demultiplexer - a circuit that selectively connects one data line to a specific output line of a group.

EQUIPMENT REQUIRED

F.A.C.E.T. base unit
Multimeter
Oscilloscope, dual trace
DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board

NOTES

Exercise 1 – Data Selector and Multiplexer

EXERCISE OBJECTIVE

When you have completed this exercise, you will have a working knowledge of multiplexer circuits by exercising a 1-of-8 multiplexer. You will gain this knowledge by exercising a 1-of-8 multiplexer.

DISCUSSION

- The 74LS151 data selector/multiplexer is a monolithic intergrated circuit with full on-chip binary decoding which allows the IC to select the desired data source.
- The multiplexer has 8 data input lines.
- Y and $\overline{Y}$ are complementary outputs.
- The multiplexer outputs are enabled only when $\overline{STRB}$ is low.
- Input data selection is controlled by the binary inputs applied to the data selects inputs
- The pull-up resistors ensure a proper high TTL level when two-post connectors are not inserted into a specific circuit.

NOTES

Exercise 2 – 1-Line-to-8-Line Demultiplexer

EXERCISE OBJECTIVE

When you have completed this exercise, you will have a working knowledge of a demultiplexer. You will gain this knowledge by exercising a 1-line-to-8-line demultiplexer.

DISCUSSION

- The 74LS155 data demultiplexer is a monolithic IC with full on-chip binary decoding and strobe inputs which allows the IC to route the input data to a selected output line.
- The demultiplexer has 8 output lines.
- The output select control lines select one output at a time.
- The select lines of the demultiplexer are hardwired to the output lines on the COUNTER circuit.

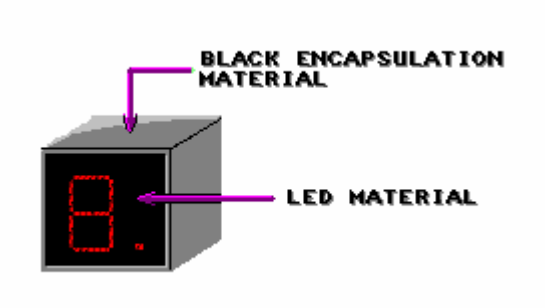
NOTES

UNIT 5 – 7-SEGMENT DRIVER/DISPLAY

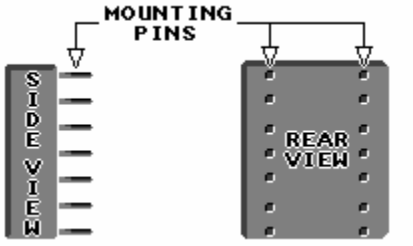
UNIT OBJECTIVE

At the completion of this unit, you will be able to control a 7-segment LED display by using a decoder/driver IC.

UNIT FUNDAMENTALS

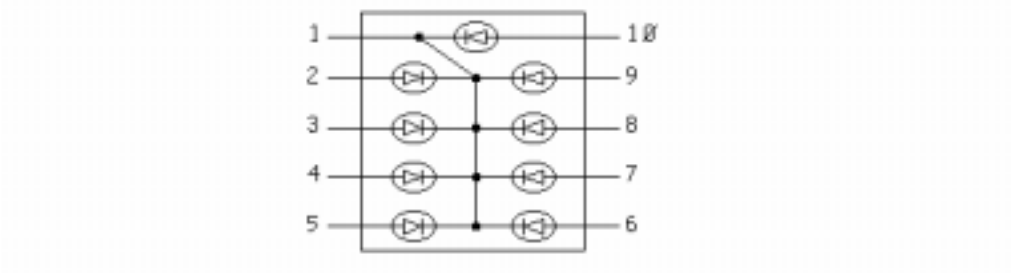


A **7-segment LED display** is constructed with 7 bars of semiconductor material capable of emitting light when stimulated by a drive voltage. The individual LEDs are encapsulated in an opaque material that serves as the device housing. In general, 7-segment displays are available in red, high efficiency red, green, or yellow. Each color denotes a specific **luminous intensity** at a given test current.

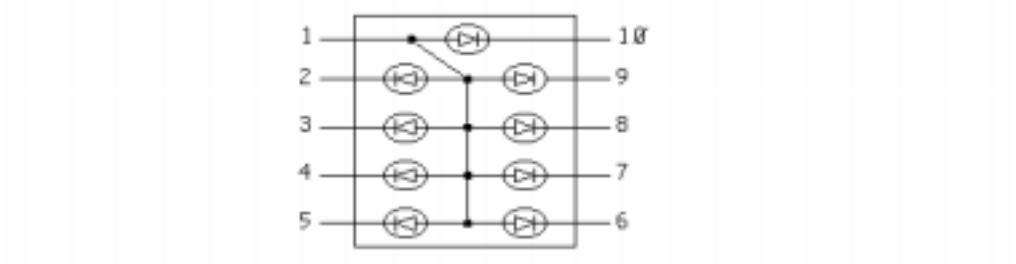


The number of pins varies with the specific IC selected. Typically, there are an equal number of pins on both sides of the dual-in-line housing.

Package dimensions are about the same as those of a dual-in-line, 14-pin TTL IC. The 7-segment display can be socket mounted or directly soldered to a PCB.

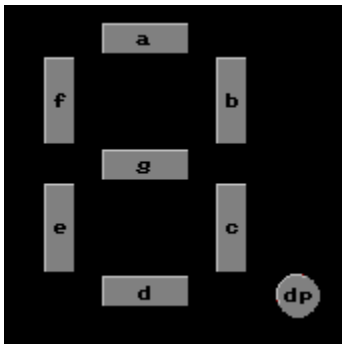


This configuration is called a **common cathode** display because all the cathodes are connected together.

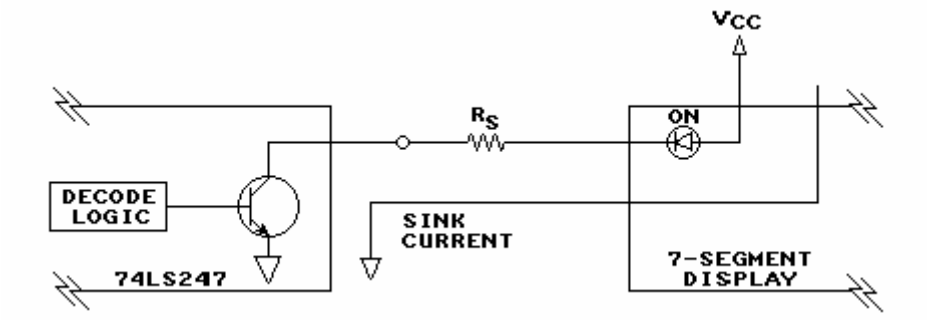


This configuration is called a **common anode** display because all the anodes are connected together.

For both configurations, the total current of the display (sum of the segment currents) flows through the common terminal of the package.

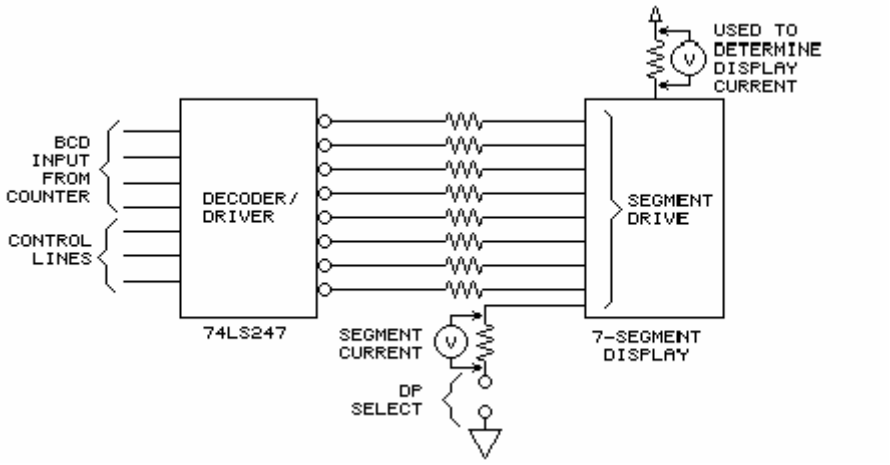


Each display segment is assigned an identifier (a through g). Groups of segments are driven to produce specific figures or symbols. For example, segments e, f, a, b, c, and g (on) produce the letter A.



The 74LS247 **decoder/driver** used in this unit drives a 7-segment (outputs a through g) display. This type of IC, a **BCD-to-7-segment decoder/driver** provides internal logic that can select (decode) the proper group of segments needed to display a given character.

The 74LS247 also provides output drivers (buffers) that supply the **sink current** for each segment of the display.



The 74LS247 uses a 7-segment display to generate the symbols 0 through 9. Although the 7-segment display can be configured to generate symbols from 0 through 9, A through F, and other unique symbols, the 74LS247 can decode only symbols 0 through 9.

You will use sensing resistors to determine display, or digit, current and segment current: I = V/R. BCD inputs (hardwired to the COUNTER circuit) and control inputs condition the 74LS247 decoder/driver. The 7-segment display indicates the equivalent BCD code applied to the decoder/driver. A two-post connector at dp select controls the dp segment.

NEW TERMS AND WORDS

7-segment LED display - an IC that can be configured to display numbers 0 through 9 and hexadecimal values A through F.
luminous intensity - specifies the light energy generated by a segment for a given test current.
common cathode - a 7-segment display with all of the cathode elements connected together.
common anode - a 7-segment display with all of the anode elements connected together.
decoder/driver - an IC that can decode a BCD input code and provide the drive current required for a 7-segment display.
BCD-to-7-segment decoder/driver - an IC designed to control an individual segment display.
sink current - the current that flows into an output pin of a driver; usually considered with a low-level TTL output.

EQUIPMENT REQUIRED

F.A.C.E.T. base unit
Multimeter
Oscilloscope, dual trace
DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board

NOTES

Exercise 1 – LED Decoder/Driver

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to operate a 7-segment decoder/driver. You will verify your results with a 7-segment display.

DISCUSSION

- The 74LS247 is a medium-scale integration (MSI) circuit that uses open collector technology to drive common anode 7-segment displays.
- The 74LS247 outputs are active low and can each sink 24mA of current.
- The BCD inputs are decoded to generate the active outputs necessary to form a proper display.
- More than one output at a time can be active.

NOTES

Exercise 2 – 7-Segment LED Display

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to use BCD codes to produce decimal equivalent displays. You will verify your results on a 7-segment display.

DISCUSSION

- A 7-segment display combines a group of LEDs into a network.
- Each driver output of the 74LS247 decoder/driver is connected to one segment of the 7-segment display through a current-limiting resistor.
- The 74LS247 BCD decoder/driver simultaneously turns on and off segments required to produce specific characters.

NOTES

UNIT 6 – PARITY GENERATOR/CHECKER

UNIT OBJECTIVE

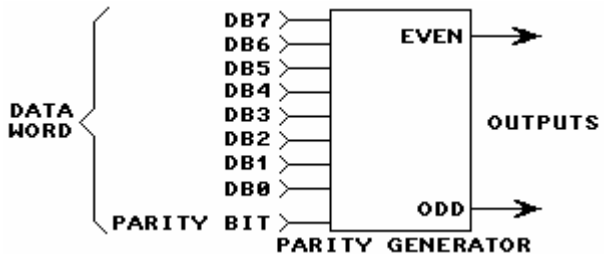
At the completion of this unit, you will be able to establish the parity of an 8-bit word by using a parity generator and checker.

UNIT FUNDAMENTALS

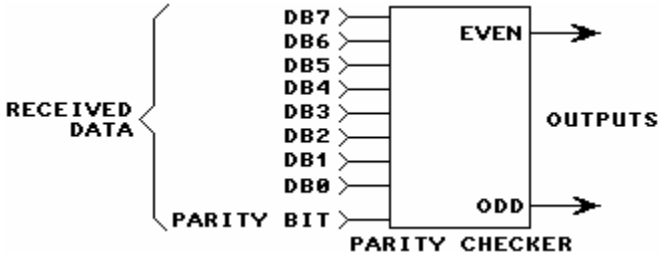
Parity refers to error detection. Computers use parity to ensure that the bit pattern of a word is not corrupted during the data transfer process. Generally, a ninth bit, called the **parity bit,** is set or reset to ensure that the correct parity of a system is maintained; therefore, an 8-bit system has a 9-bit data bus. Parity is associated with the number of **ones** present in the data word.

PARITY BIT	8-BIT DATA WORD	SYSTEM PARITY
OFF (LOW)	[0] 1010 1010	EVEN
ON (HIGH)	[1] 1010 1000	EVEN
ON (HIGH)	[1] 1010 1010	ODD
OFF (LOW)	[0] 1010 1000	ODD

Even parity systems require an even number of ones in the data word, which includes the parity bit. **Odd parity** systems require an odd number of ones in the data word, which includes the parity bit. Because the data word, $AA for example, determines the 8 bits of the word, the parity bit is set high or low to ensure that the data word matches the **system parity**.



In this parity generator and for an even parity system, the parity bit input is set or reset to ensure that the even output is high (odd output low). For an odd parity system, the parity bit input is set or reset to ensure that the odd output is high (even output low).



In this parity checker, the even output is high if an even number of ones is present in the received data. The odd output is high if an odd number of ones is present in the received data.

NEW TERMS AND WORDS

Parity - refers to an error-checking system that ensures the integrity of data.
parity bit - refers to the ninth bit in an 8-bit data bus system.
even parity - requires an even number of ones in the data path.
odd parity - requires an odd number of ones in the data path.
system parity - specifies the expected number of ones in received or transmitted data.

EQUIPMENT REQUIRED

F.A.C.E.T. base unit
Multimeter
Oscilloscope, dual trace
DIGITAL CIRCUIT FUNDAMENTALS 2 circuit board

NOTES

Exercise 1 – Odd and Even Parity

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to generate and check the parity of 8-bit data. You will verify your results with a parity generator/checker.

DISCUSSION

- A parity generator provides an output signal that assigns an odd or even tag to a data word.
- A parity checker determines if a data word has even or odd parity.
- The parity IC has nine input lines and two active high output lines.
- The MSB input controls the level at input I of the parity IC, simulating a ninth, or parity bit.
- DATA controls the input to the shift register.
- The summation determines whether the data word has even or odd parity.

NOTES

APPENDIX A – SAFETY

Safety is everyone's responsibility. All must cooperate to create the safest possible working environment. Students must be reminded of the potential for harm, given common sense safety rules, and instructed to follow the electrical safety rules.

Any environment can be hazardous when it is unfamiliar. The F.A.C.E.T computer-based laboratory may be a new environment to some students. Instruct students in the proper use of the F.A.C.E.T equipment and explain what behavior is expected of them in this laboratory. It is up to the instructor to provide the necessary introduction to the learning environment and the equipment. This task will prevent injury to both student and equipment.

The voltage and current used in the F.A.C.E.T Computer-Based Laboratory are, in themselves, harmless to the normal, healthy person. However, an electrical shock coming as a surprise will be uncomfortable and may cause a reaction that could create injury. The students should be made aware of the following electrical safety rules.

1. Turn off the power before working on a circuit.
2. Always confirm that the circuit is wired correctly before turning on the power. If required, have your instructor check your circuit wiring.
3. Perform the experiments as you are instructed: do not deviate from the documentation.
4. Never touch "live" wires with your bare hands or with tools.
5. Always hold test leads by their insulated areas.
6. Be aware that some components can become very hot during operation. (However, this is not a normal condition for your F.A.C.E.T. course equipment.) Always allow time for the components to cool before proceeding to touch or remove them from the circuit.
7. Do not work without supervision. Be sure someone is nearby to shut off the power and provide first aid in case of an accident.
8. Remove power cords by the plug, not by pulling on the cord. Check for cracked or broken insulation on the cord.